DIGITAL INDUSTRIES SOFTWARE

Reduce 3D IC design complexity with early package assembly verification

Executive summary

2.5D and 3D ICs present unique challenges to physical verification because they are composed of multiple chiplets of different materials integrated in all three dimensions. 3D IC designers can use Calibre Shift Left solutions to help optimize 3D IC designs and perform physical verification earlier in the flow, when assembly issues are easier to find and fix.

The Calibre Shift Left solutions support a comprehensive 3D IC verification strategy that brings trusted Calibre physical verification to the design and assembly stages so 3D IC designers can quickly find optimal choices for assembly types and device placements. Early assembly verification can also be expanded as each component matures to enable accurate signoff-level verification and final electrical signoff analysis. This approach reduces the number of verification runs, simplifies debug and instills confidence in a working, reliable 3D heterogeneous assembly design.

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2.5/3D IC designs

Unlike integrated circuit (IC) designs, multi-dimensional 2.5D and 3D ICs are composed of multiple individual chiplets, each of which may be built to a separate process node best suited for the specific purpose. There are many different design options for connecting these chiplets: chiplets connected via interposer with bump connections and through-silicon-vias (TSVs), chiplets on package, chiplets on packages with discreet and thinned interposers embedded without TSVs, chiplets stacked on chiplets through direct bonding techniques, chiplets stacked on chiplets with TSVs or copper pillars and more bumps...and the list goes on. Further, any or all of these approaches can be combined on a single 3D IC assembly (figure 1). This flexibility results in multiple components of different materials integrated in all three dimensions, which creates new and unique verification challenges for 2.5/3D IC designers.

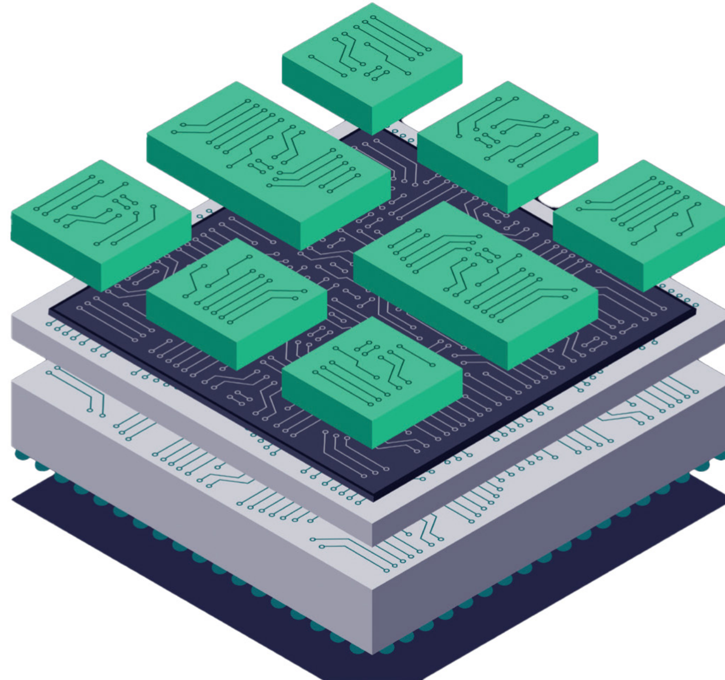

Figure 1. 3D IC assemblies can use a variety of designs.

3D IC assembly flow

Multi-dimensional ICs are one part of the industry's answer to moving beyond the limits of Moore's law. While 2.5D approaches, particularly chiplets placed upon a silicon interposer, have gained broad adoption, the move to true 3D IC is still early in its design lifecycle. Design tools and best design practices continue to evolve and improve, but many challenges are yet to be resolved. In general, these advanced design approaches all require some similar steps. First, traditional IC design requires some method to disaggregate the components of a design into appropriate chiplets. Each chiplet must then be assigned to an appropriate foundry technology process node. Next, decisions must be made about which of the many different types of 3D IC designs best serve the intended market purpose. In a true 3D IC, this can be a challenging task, as the specific approach, materials, and chiplet placements used will induce thermal and mechanical stresses that can impact the intended electrical behavior of the full assembly design. Selecting the optimal approach and optimal chiplet placements becomes critical, implying multiple iterations will be required to determine the best final design.

3D IC physical verification

Novel challenges exist when it comes to physical verification (PV) of 2.5/3D IC designs. A typical 2.5/3D IC PV flow starts with dedicated verifications of each chiplet against their assigned foundry process requirements. In one sense, this is similar to verifying routed blocks independently before incorporation into a full system-on-chip (SoC) design. Where 3D IC PV diverges more vigorously from a traditional SoC PV flow is in the full assembly verification. For layout vs. schematic (LVS) verification, a source netlist is needed. Historically, the assembly netlist takes the form of a comma-separated value (CSV) spreadsheet, where each pin is listed with its coordinates, a pin

specific name, and the name of the assembly-level net to which it is associated. This netlist is typically created manually, introducing a great deal of uncertainty with the possibility of human error. When it comes to verification, the most common approach for checking physical and electrical compliance for a 3D IC requires the use of separate rule decks for design rule checking (DRC), LVS, etc. for each interface within the package (chip-to-chip, chip-to-interposer, chip-to-package, interposer-to-package, etc.). These rule decks typically use pseudo-devices, commonly in the form of 0 ohm resistors, to identify the connections across each interface while still preserving the individual chiplet-level net names.

However, the multiple deck approach creates its own set of challenges. Designers must associate the many individual rule decks to the corresponding interfaces within the assembly layout, which may not always be intuitive. As errors are identified, designers must be able to highlight them at the proper interfaces (with proper handling of rotations and magnifications) to help identify the appropriate fixes. With multiple dedicated rule decks and verification runs, keeping track of which results correspond to which interfaces and having confidence that the full assembly is correct is again time-consuming and wrought with the possibility of human error.

The use of pseudo-devices also presents additional challenges to designers, the first being how to introduce these pseudo-devices into the schematic or source netlist. This insertion is often manually performed, introducing yet more risk of human error. Pseudo-devices can also cause issues with the LVS checking at the interfaces to ensure correspondence to the layout. From a debug perspective, when there are connection issues, the separation created by such devices makes it difficult to properly trace the full connectivity across chiplets. In other words, the connected net between two chiplets is still seen as two separate nets, making probing (and ultimately debug) difficult. Finally, the presence of these pseudo devices, even 0 ohm resistors, can have unintended impacts when it comes to static timing analysis tools, as a single connection is again seen as two separate nets that must be passed into Verilog.

Finally, the use of these interface rule decks (particularly for LVS and subsequent electrical analyses) makes it practically impossible to generate a full assembly post-layout netlist or to otherwise understand electrical interactions across multiple

components. For example, consider checking for adequate protection devices against electrostatic discharge (ESD) using an electronic design automation (EDA) tool like the Calibre® PERC™ reliability platform. Without a holistic assembly approach, it is impossible to verify ESD protection when the ESD circuits exist in one chip and the protection devices exist in another. Similarly, like a traditional SoC, assembly approaches to metallization from packaging or backside metal can create charge that may create antenna impacts. Given these metals may ultimately connect to multiple chiplets of heterogeneous processes, how can assembly designers possibly verify and protect against such yield and reliability issues using interface-only rule decks?

Shift left IC design and verification

To bring more advanced IC designs to market faster, and achieve the ramp to volume production sooner, Calibre Design Solutions provides tools and functionalities that enable design companies to implement “shift left” physical verification and design optimization earlier in their design and implementation flows (figure 2).

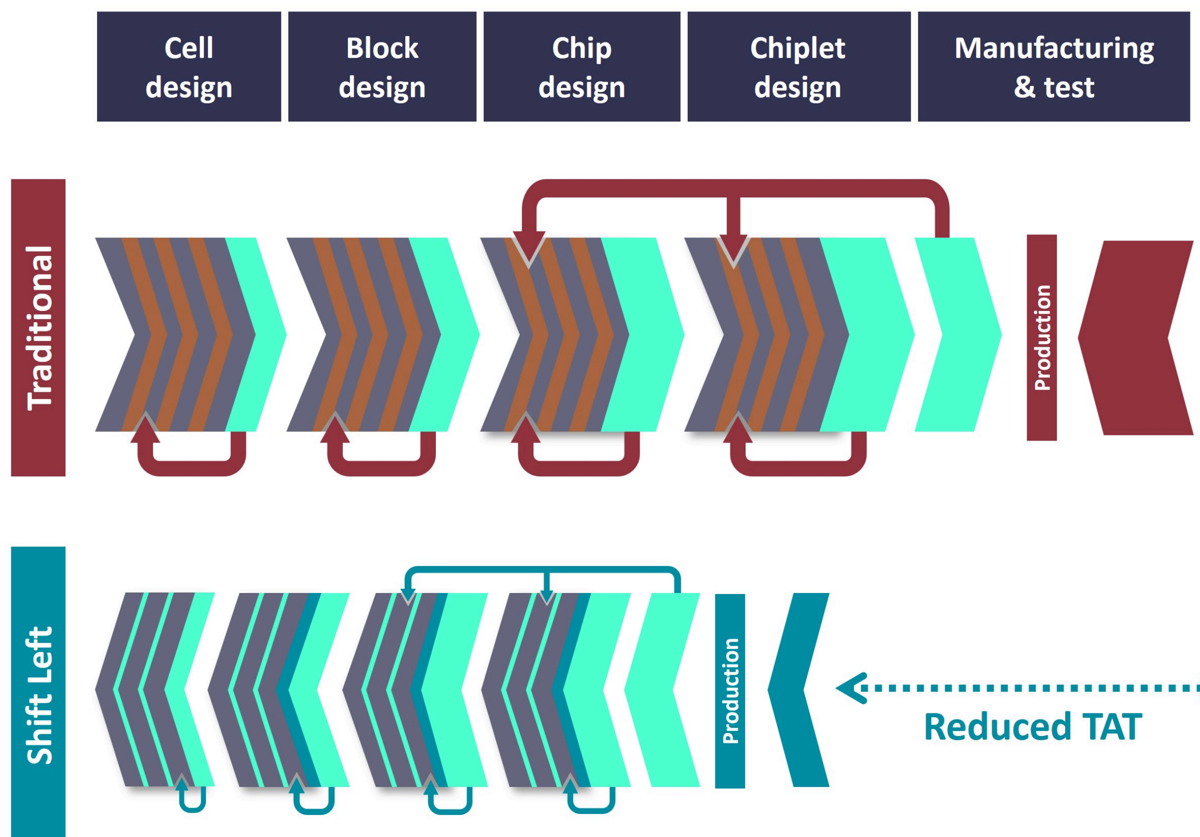

Figure 2. Calibre Shift Left design solutions enable design teams to enhance productivity and design quality while reducing time to market.

At Siemens EDA, we collaborate with design companies and foundries every day to understand what designers need and want to achieve business and design goals, and to provide an electronic design automation (EDA) ecosystem that supports every designer where they are with the tools they need. While many of the physical verification challenges facing 3D IC designers are unique to multi-dimensional designs, the same tools and functionalities can be applied to enable 3D IC design teams to perform accurate and efficient physical verification on these assemblies.

Using the trusted Calibre nmPlatform in conjunction with other tools from the Siemens EDA portfolio, 2.5/3D IC design teams have the freedom and flexibility to create a best-in-class shift left solution that improves designer productivity and

design quality, provides faster runtimes and increased resource efficiency, and allows their designers to work within familiar design and implementation environments, all while achieving Calibre confidence throughout the design implementation flow.

Shift left for 3D IC physical verification

It is clear that true 3D IC verification of physical and electrical constraints requires a holistic assembly-level approach. Enabling such an approach requires adherence to appropriate design stage requirements. 3D IC designers, like IC/SoC designers, have options that help them optimize their 3D IC designs and perform physical verification earlier in the 3D IC flow, enabling them to find and eliminate assembly issues when changes are easier to apply.

First, using a tool like the Siemens Xpedition™ Substrate Integrator (XSI) software, 3D IC designers can specify several different kinds of 3D floorplans. While not all the detail for all the layers and materials will be available, it is still sufficient for early analysis to help rule out configurations that contain serious flaws. Using uniform materials, and simplified (or even uniform) power maps, designers can at least eliminate some design configurations from consideration.

A holistic approach requires full knowledge of both the 3D IC assembly and the individual chiplet processes. The most obvious challenge is how to ensure that the active chiplets in a 3D IC assembly will behave electrically as intended. Of course, LVS-level verification requires an assembly-level source netlist. Designers can create this netlist using automated approaches in the form of Verilog, or generate it from traditional package tools in other industry-standard formats. In Calibre verification, this issue is addressed by extending the already widely adopted infrastructure in place with the Calibre 3DSTACK tool to generate an assembly description that defines the 3D stackup using the Calibre 3DSTACK+ tcl text-based format. For complex

assemblies, this description generation can be automated using such tools as the XSI design planning tool. Alternatively, newer formats such as the 3Dblox™ standard can also encapsulate such information.

With these options, a true 3D IC physical verification approach becomes possible. This knowledge of the stack-up allows the Calibre engine to understand the connectivity and geometric interfaces across all components in the assembly, enabling a single deck and single run to not only identify and display DRC and LVS issues in a single results output, but also use the data captured during the individual chiplet-level LVS and similar runs, combined with the top assembly-level extraction data, to generate a post-assembly netlist for further analysis. This understanding of the assembly can also drive automation of cross-die parasitic coupling impacts and enable full assembly analyses, including not only ESD and antenna issues, but also extending to capture thermal and mechanical stress impacts on the 3D IC electrical behavior.

Every designer knows that mechanical stresses and temperature changes can affect electrical behavior. These impacts apply to active devices, changing device mobilities and conductivities, as well as to passive devices, impacting resistivities and electromigration (EM) impacts. In a traditional IC/SoC design, these impacts are largely safeguarded by the fact that all devices are on a common silicon die. With a few appropriate design rules to keep devices sufficiently separated from local impacts, most issues are avoided. By extracting some additional device parameters, further gross deficiencies can be flagged for review, and enabling any additional concerns can be captured during post-layout simulation. Unfortunately, when it comes to the world of 3D IC design, those safeguards are no longer practical.

2.5/3D IC assemblies introduce new mechanical and heat stresses, while also impacting access to thermal heat sinks. New thermal impacts come from providing power and active device toggling, we well as from the manufacturing processes. These new sources of stress create new verification challenges for 3D IC design.

The first step is to create the initial power network. The Siemens mPower™ solution can pull from the generated output of the Calibre 3DSTACK run to obtain the connectivity and any coupling across the chiplets. Adding the individual chiplet networks and internal connectivity to this data enables the creation of power maps that can be used to drive the thermal analysis.

3D IC thermal analysis can be performed using Calibre 3DThermal technology. Using the same assembly definition created for the Calibre 3DSTACK connectivity extraction, together with appropriate materials property definitions for each component, as well as any boundary conditions, the Calibre 3DThermal tool can leverage the widely-adopted Simcenter™ Flotherm™ thermal solver, generating the thermal maps needed. Because the Calibre engine has all the detailed layer information for the individual chiplets, it can generate very accurate individual die thermal models. Additionally, by leveraging the chiplet-specific layout and connectivity, those thermal impacts can be transformed to the device-level, enabling accurate post-assembly simulations or EM and voltage (IR) drop analysis.

Similarly, innovative capabilities in the Calibre toolsuite enable the capture of the electrical impacts of all stresses on the active chiplets. Using the same assembly stack-up definition used for the initial Calibre 3DSTACK runs and adding corresponding mechanical stress properties for each of the materials across the full assembly enables 3D IC designers to generate a stress map. As in the case of the thermal analysis, these stresses can then be pushed down to the device level to enable accurate post-assembly simulation and analysis at the active chiplet levels.

Unfortunately, these impacts cannot be treated in isolation. Mechanical stresses induce heat. Thermal impacts create mechanical stress. Both thermal and mechanical stress impact the electrical behavior, which can, in turn, generate more heat. These impacts can be largely identified and mitigated through iteration. A power map can be used to drive extraction of a thermal map. A thermal map can be passed to augment the stress maps. The stress and thermal impacts can be passed to device-level netlists for simulation or updated EMIR analysis, etc. Ultimately, this level of cross-simulation can be automated for the user.

However, the challenges of 3D IC verification don't stop there. If this final signoff level of accuracy is performed at the final steps of assembly and an issue is identified, it is essentially too late to make sufficient modifications to the assembly to address them. How can 3D IC designers identify and address these issues earlier in the design flow? Further, how can 3D IC designers make optimum choices for the 3D IC floorplan that will create the best possible electrical behavior?

As design components begin to mature, with chiplet or interposer-level DEF data and generic published materials properties, further iterations can become more accurate. As individual chiplets or interposers have their full layout, more detailed models can be generated. Further, at least for thermal impacts, designers can capture thermal maps for pre-existing chiplets or sub-assemblies in standard formats like ECXML, ultimately simplifying and speeding the analysis required when the chiplets or sub-assemblies are placed in context of the full assembly. Using this approach, designers should not encounter many (if any) unwanted surprises by the time final iteration is performed.

This early assembly verification can not only help 3D IC assembly designers hone in earlier on the best choices for assembly types and device placements, but can also be expanded as each component matures to enable accurate signoff-level verification. With such an approach, the number of verification runs is reduced, debugging is greatly simplified, the total number of iterations are greatly reduced, and ultimately, assembly designers achieve early confidence in a working, reliable 3D heterogeneous assembly design.

Conclusion

It's clear that true 3D IC analysis and verification requires comprehensive knowledge of the entire system at the detailed level of each component. By enabling such an environment early in the assembly flow, not only is the verification approach itself greatly simplified and made faster, but also an innovative approach for multi-physics

challenges can be accommodated. The Calibre Shift Left solutions, in conjunction with other Siemens EDA tools, support a comprehensive 3D IC verification strategy that uses proven and trusted functionality to ensure accurate results. Implementing this approach during early design and assembly stages helps 3D IC designers identify the optimal solution across the many different 3D IC offerings and expand assembly physical verification to both early design stages and final electrical signoff analysis.

IP designers and block/chip designers can also take advantage of Calibre Shift Left solutions for their unique verification challenges.

For more details about the full range of Calibre Shift Left solutions, and the tools and strategies available, visit our Shift left with Calibre solutions page. The shift left resource library provides direct access to papers, videos, and other shift left resources.

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John Ferguson is the product management director for Calibre DRC applications at Siemens Digital Industries Software. John has extensive experience in the area of physical design verification. He holds a B.Sc. degree in Physics from McGill University, an M.Sc. in Applied Physics from the University of Massachusetts, and a Ph.D. in Electrical Engineering from the Oregon Graduate Institute of Science and Technology.

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