

# How to Achieve Ultrafast Power Supply Transient Response for RF Applications

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## Abstract

This article presents practical methods for achieving an ultrafast power supply transient response in wireless and, especially, RF applications. It aims to resolve the system designer's challenge of low signal processing efficiency caused by the power supply transient blanking period. Example solutions are presented for different applications. The Silent Switcher® 3 monolithic power family is introduced for the best transient performance.

## Introduction

Signal processing units and system-on-a-chip (SoC) units usually possess abruptly changing load transient profiles. This load transient will result in a disturbance on the supply voltage that is critical in radio frequency (RF) applications, as the clock frequency will be highly affected by the varying supply voltage. As a result, RFSocS usually apply blanking time during the load transient. In 5G applications, information quality is highly related to this blanking period during the transition. Thus, there is an increasing need to minimize the load transient effect on the power supply side to improve the system-level performance for any RFSoc system. This article will introduce several methods used in RF applications to achieve fast transient response in a power supply design.

## Fast Transient Silent Switcher 3 Family for RF applications

One of the most straightforward methods to achieve fast transient power rails is to select regulators that feature fast transient performance. The Silent Switcher 3 family of ICs features exceptionally low frequency output noise, fast transient response, low EMI emissions, and high efficiency. It features an ultrahigh performance error amplifier design that can provide extra stabilization even with an aggressive compensation. The 4 MHz maximum switching frequency enables the IC to push the control loop bandwidth to the mid-hundred kHz range in a fixed frequency peak current control mode. The Silent Switcher 3 ICs that designers can select to achieve fast transient performance are listed in Table 1.

**Table 1. Silent Switcher 3 Family Parameters**

Part No.	Current Level	Package	Temperature Rating	Feature
LT8625S	8 A	20-lead, 4 mm × 3 mm LQFN	125°C	Ultralow noise, fast transient
LT8625SP	8 A	20-lead, 4 mm × 3 mm LQFN	150°C	Ultralow noise, fast transient, top side cooling
LT8625SP-1	8 A	24-lead, 4 mm × 4 mm LQFN	150°C	Ultralow noise, fast transient, top side cooling
LT8627SP	16 A	24-lead, 4 mm × 4 mm LQFN	150°C	Ultralow noise, fast transient, top side cooling

Figure 1 shows a typical 1V output power supply based on the LT8625SP for the 5G RFSoc, which needs fast transient response and low ripple/noise level at the same time. The 1V load consists of both transmitted/received related circuits as well as local oscillators (LOs) and voltage controlled oscillators (VCOs). The transmitted/received loads see abrupt load current change in the frequency division duplex (FDD) operation. At the same time, LOs/VCOs see constant load but require critical high accuracy and low noise. The high bandwidth feature of LT8625SP enables designers to power the two critical 1V load groups from a single IC by separating the dynamic load and static load with a second inductor (L2). Figure 2 shows the output voltage response with a 4 A to 6 A dynamic load transient. The dynamic load recovers within 5  $\mu$ s with less than 0.8% peak-to-peak voltage, which minimizes the effect on the static load side with a less than 0.1% peak-to-peak voltage. This circuit can be modified to accommodate other output combinations, like 0.8 V and 1.8 V, that can all directly supply the RFSoc load without the LDO regulator stage due to the ultralow noise in the low frequency range, low voltage ripple, and ultrafast transient response.

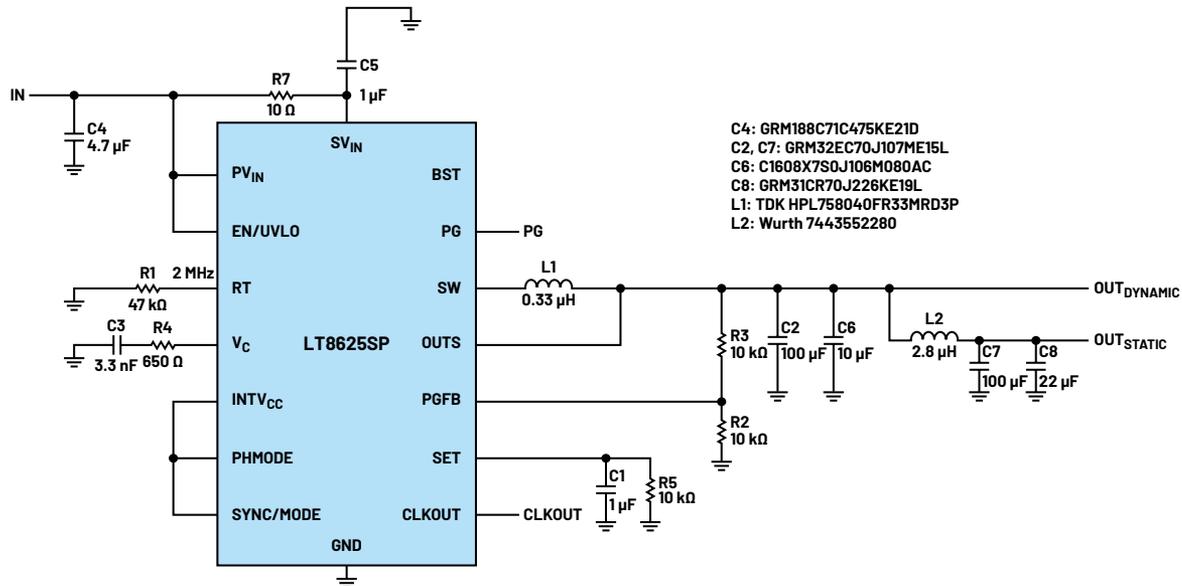


Figure 1. Typical application circuits for LT8625SP in dynamic/static separated RF loads.

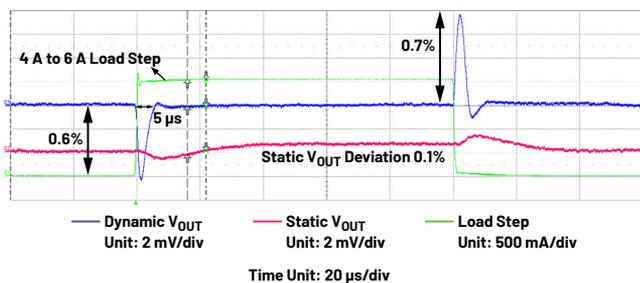


Figure 2. Load transient response is fast with minimum  $V_{OUT}$  deviation and won't affect the static load.

In time division duplex (TDD) mode, the noise critical LOs/VCOs become loaded and unloaded together with the transmit/receive mode changes. Thus, a simplified circuit as shown in Figure 3 can be used as all of the loads are considered to be dynamic load while a more critical postfiltering is required to maintain the low ripple/low noise feature for the LOs/VCOs. A 3-terminal capacitor in feed-through mode can be used to achieve enough postfiltering with a minimized equivalent L that maintains a fast bandwidth for the load transients. The feed-through capacitor together with the remote side output capacitors forms two more LC filter stages while all the Ls come from ESLs of the 3-terminal capacitor, which is very small and less harmful to the load transient. Figure 3 also illustrates an easy remote sensing connection for the Silent Switcher 3 family. Due to the

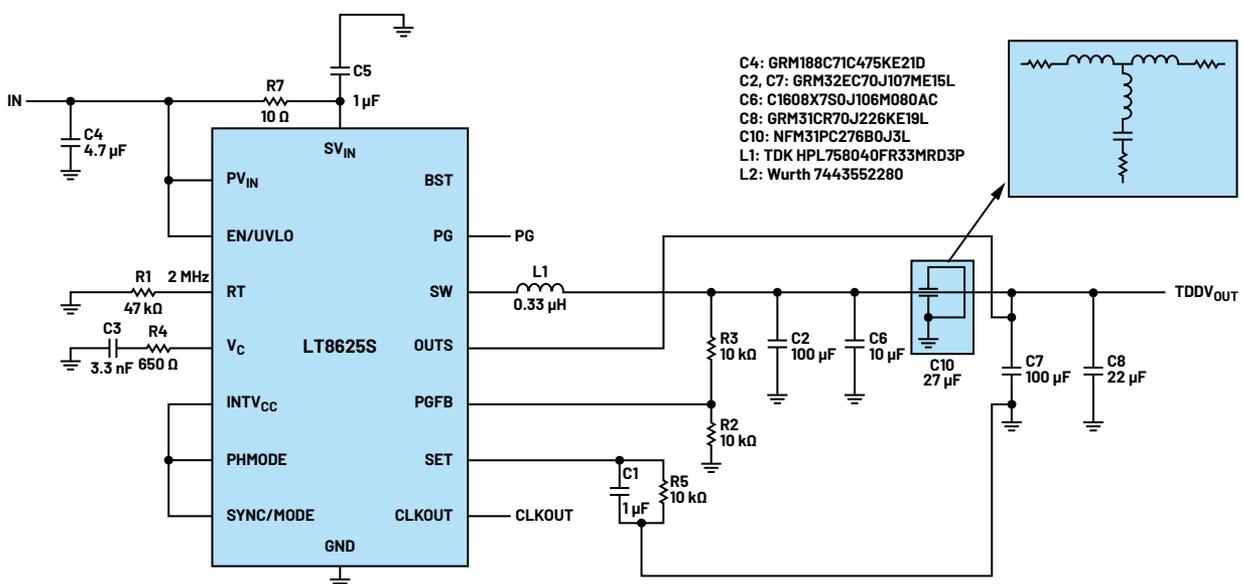


Figure 3. Typical application circuit for LT8625SP in dynamic/static combined RF loads.

unique reference generation and feedback technology, one only needs to Kelvin connect the SET pin capacitor's (C1) ground and the OUTS pin to the desired remote feedback point. No level shifting circuits are needed for this connection. Figure 4 shows a 1 A load transient response waveform with <math><5 \mu\text{s}</math> recovery time and <math>< 1 \text{ mV}</math> output voltage ripple.

### Precharge Signals Drive Silent Switcher 3 Family for Fast Transient Response

In some cases, the signal processing unit is powerful with enough GPIOs, and the signal processing is well scheduled as the transient event can be known ahead of time. This usually happens in some FPGA power supply designs where the precharge signal can be generated to help power the supply transient response. Figure 5 shows a typical application circuit using the precharge signal generated by the FPGA to provide a bias before the real load transition happens so that the LT8625SP can have extra time to accommodate the load disturbance without too large of a  $V_{\text{OUT}}$  deviation and recovery time. The tuning circuit from FPGA's GPIO to the input of the inverter has been omitted as the precharge signal is acting as a disturbance on the feedback. The level is controlled to be 35 mV. Moreover, to avoid the precharge signal effect on the steady state, a high-pass filter is implemented between the precharge signal and the OUTS. Figure 6 shows a 1.7 A to 4.2 A load transient response waveform. The precharge signal is applied to the feedback (OUTS) ahead of the real load transient, whereas less than 5  $\mu\text{s}$  recovery time is achieved.

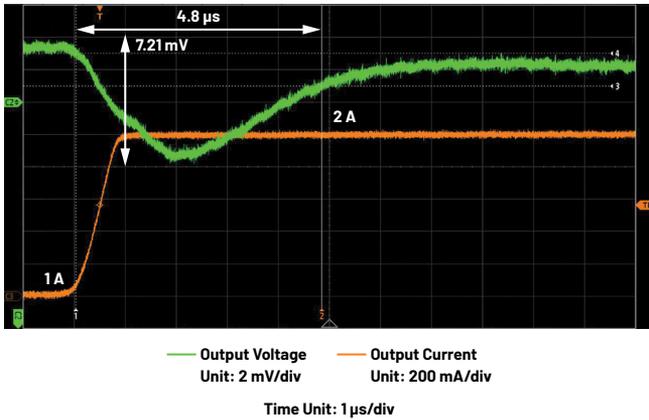


Figure 4. Feedthrough capacitor boosts transient response while maintaining minimized output voltage ripple.

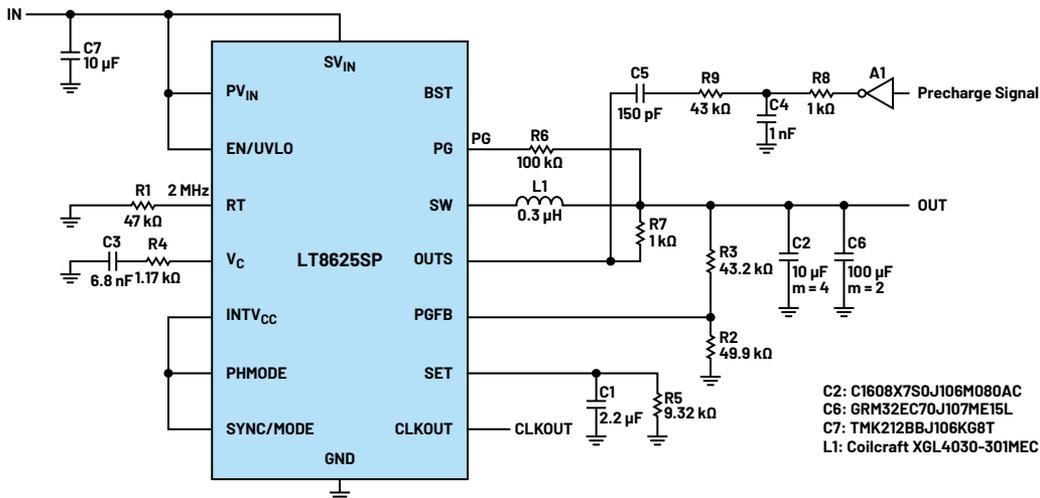


Figure 5. T8625SP with a precharge signal fed into OUTS pin to achieve fast transient response.

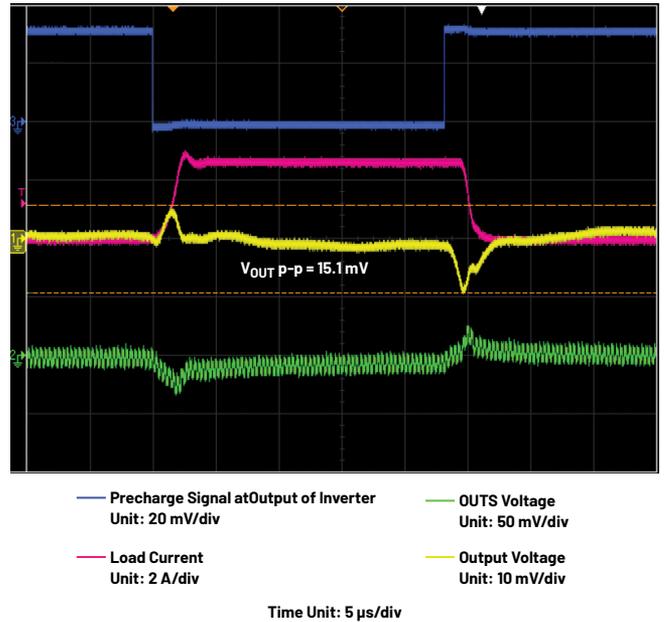


Figure 6. LT8625SP feedback affected by both the precharge signal and the load transient achieving a fast recovery time.

### Active Drooping on Circuit for Ultrafast Recovery Transient

In beamformer applications, the supply voltage changes all the time to accommodate different power levels. As a result, the accuracy requirement for the supply voltage is usually 5% to 10%. In this application, stability is more important than the voltage accuracy as a minimized recovery time during the load transient will maximize the data processing efficiency. A drooping circuit perfectly fits into this application as the drooping voltage will reduce or even eliminate the recovery time. Figure 7 shows the schematic for an active drooping circuit for the LT8627SP. An extra drooping resistor has been added between the error amplifier's negative input (OUTS) and the output (VC) to maintain a steady state error in the feedback control loop during the transient. The drooping voltage can be expressed as:

$$\Delta V_{\text{DROOP}} = \frac{R_7}{R_7 + R_8} \times \left( \Delta V_{\text{OUT}} - \frac{\Delta I_{\text{OUT}}}{g} \right) \quad (1)$$

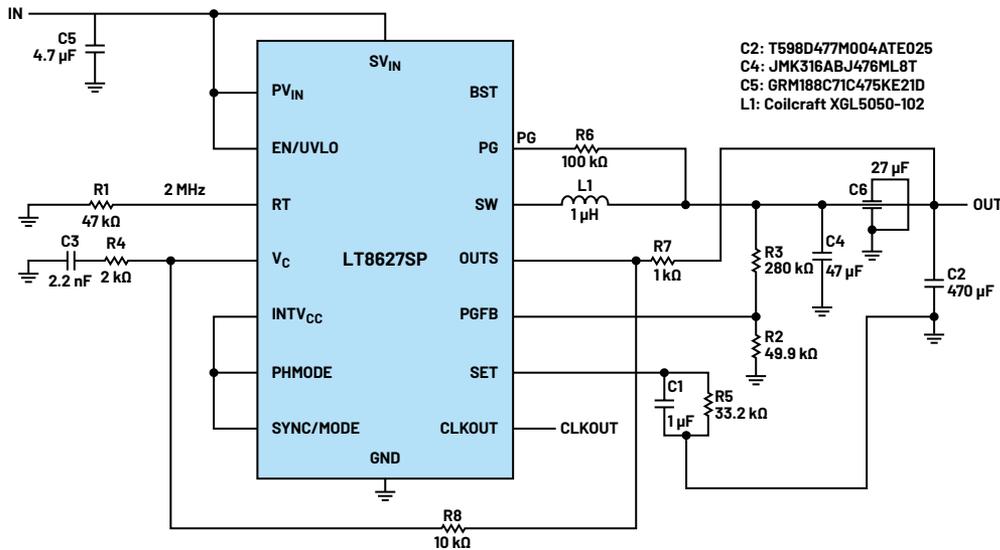


Figure 7. LT8627SP with an active drooping resistor placed between OUTS and VC to achieve a fast transient recovery time.

Whereas  $\Delta V_{OUT}$  is the initial voltage variation caused by the load transient,  $\Delta I_{OUT}$  is the load transient current, and  $g$  is the VC pin to switch current gain. In designing the drooping circuit shown in Figure 7, special considerations need to be taken:

- ▶ The drooping current should not exceed the VC pin current limit. For LT8627SP's error amplifier output, it is proper to limit the current to below 200  $\mu$ A to avoid saturation and this can be achieved by changing R7 and R8 values.
- ▶ The drooping voltage needs to accommodate the output capacitance so that the voltage deviation during the transient is on a similar level of the drooping voltage to achieve minimum recovery time during the transient.

Figure 8 shows typical waveforms for the above-mentioned circuit during a 1 A to 16 A to 1 A load transient. It is worth noticing that now the 16 A to 1 A load transient speed is no longer bottlenecked by the bandwidth but by the minimum on time of the regulator.

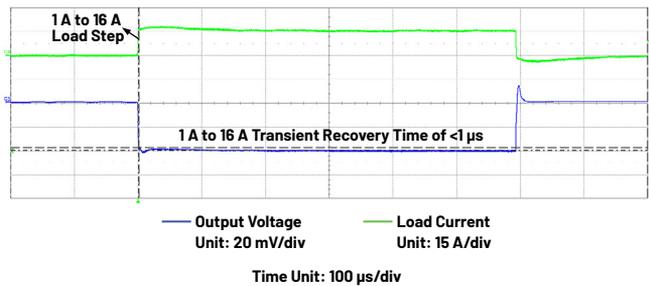


Figure 8. Droop transient response can be achieved to minimize the transient recovery time for LT8627SP.

## Conclusion

The wireless RF field is becoming increasingly calculation dependent and sensitive to the transient response time due to the time critical nature of the high speed signal processing. System design engineers face challenges to increase the power supply transient response speed so that the blanking time can be minimized. The Silent Switcher 3 family is the next-generation of monolithic regulators optimized for noise sensitive, intensive dynamic load transient solutions in wireless, industrial, defense, and healthcare fields. Based on the load conditions, special techniques and circuits can be applied to further improve the transient response.



## About the Author

Xinyu Liang is the applications engineering manager in the Industrial and Multimarket Group at Analog Devices focusing on power products. He received his Ph.D. degree in electrical engineering in 2018 from North Carolina State University and he started his career at ADI in 2019 after graduation.